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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 15

Application Number: 09/987,566
Filing Date: November 15, 2001
Appellant(s): MORISHITA, FUKASHI

Alexander V. Yampolsky
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 10 June 2003.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief provides claims 19-20 in one group to stand or fall together.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 19 and 20 are rejected under 35 U.S.C. §102(e) as being anticipated by Bion et al. (USPN 5,862,091). Bion discloses, in Figs. 11 and 12, a circuit comprising: "a first voltage (inverting input of 37, i.e., gate of 40)"; "a second voltage (non-inverting input of 37, i.e., gate of 39)"; "a first insulated gate transistor (40)"; "a second insulated gate transistor (39)"; "a power supply voltage (Vcc, provided by way of transistor 36)"; "a reference voltage (the "internal voltage generated from said power supply (Vcc)", provided to the non-inverting input of 37 by way of resistor-connected transistor 38)"; an "operation current supply (39 and 40)"; and "a buffer circuit (44)", all connected and operating similarly as recited by Applicant. Reference is made to Col. 8, lines 45-56 and claim 8 of Bion et al. which discloses that 39 and 40 are different sizes.

(11) Response to Argument

It is noted that it appears that "38" in line 12 of page 6 should be --36--.

In the paragraph linking pages 6-7, Appellant argues that "the output of the comparator 37 (of Bion) does not produce a difference signal corresponding to the difference between the power supply Vcc and the reference voltage Vcc". This statement is not understood because

nowhere does the claim recite that the "difference signal" corresponds "to the difference between the power supply Vcc and the reference voltage Vcc". Claim 19 states "said difference signal corresponding to a difference between the first and second voltages". The rejection clearly provides that the "first voltage" is being read as the "inverting input of 37" and the "second voltage is being read as the "non-inverting input of 37". Element 37 of Figs. 11 and 12 is a comparator. The purpose of a comparator is to provide a difference signal corresponding to the difference between the voltages on the inverting and non-inverting terminals. Note this is precisely the operation of Appellant's comparator (e.g., Fig. 4), which has substantially the same structure as Bion.

Appellant's discussion concerning the "power supply voltage" and the "reference voltage" is not understood. All that the claims state about the "power supply voltage" is that the "first insulated gate transistor" receives the "power supply voltage". Clearly, in the reference to Bion, the gate of the "first insulate gate transistor (40), which corresponds to the inverting input, receives the power supply voltage Vcc when transistor 36 turns on. This operation is seen to meet the claim language. Additionally, all that the claims state about the "reference voltage" is 1) that the "second insulated gate transistor" receives the "reference voltage" and 2) that the reference voltage" determines the "level of an internal voltage generated from said power supply". Firstly, as seen in Bion, the gate of the "second insulate gate transistor (39), which corresponds to the non-inverting input, receives a voltage at the drain of transistor 38. This operation is seen to meet the claim language. And secondly, it is clear that the voltage on the drain of 38 determines the "voltage level" on the non-inverting input and that this voltage is an "internal voltage" generated from the "power supply voltage" Vcc.

Appellant further argues that "the output of 37 produces the read out data supplied to the inverter input". Examiner agrees that the output of 37 is the inverse of the voltage provided to the inverting input. And clearly, the voltage at the output of 37 is the difference between the voltages at the inverting and non-inverting inputs, i.e., the "first and second inputs".

The relevance of the discussion in lines 1-3 of page 7 is not understood.

Contrary to Appellant's arguments the first full paragraph of page 7, the reference to Bion is seen to meet the claim limitation for the reasons discussed above.

In the second full paragraph of page 7, Appellant's arguments are not seen to be relevant or relate to any claim language. Whether or not transistor 38 of Bion et al. provides compensation for transistor 36 is not seen to have any relevance to the issues at hand.

In the third full paragraph of page 7, Appellant's conclusions can only be seen to be erroneous. Firstly, transistors 36 is not always on, unlike transistor 38, therefore the voltage at the inverting inputs will not always be the same as the voltage at the non-inverting input. And secondly, Appellant's conclusion that no comparison is performed when the inputs to comparator 37 are the same is seen to be without basis. Element 37 is a comparator. A comparator will necessarily compare the voltage at both inputs, even if the values of inputs are the same. Further, since the sizes of transistors 39 and 40 are different, comparator 37 will necessarily provide a result when the input values are the same.

In the fourth and fifth full paragraphs of page 7, Appellant argues that "Bion et al. does not disclose a detection signal indicating whether the power supply voltage is higher than the reference voltage that determines the internal voltage generated from the power supply voltage". Again, nowhere is this limitation found in the claims. The claim states that the "buffer"

generates "a binary level detection signal whether the first voltage is higher than said second voltage". Since element 44 is a high gain (i.e., infinite gain) amplifier, it would be more than reasonable to consider such to be a buffer circuit. Further, since element 37 is a comparator, it necessarily will provide an indication when the "first voltage", the inverted input, is higher than the "second voltage", the non-inverted input. Further, this indication will be passed through buffer 44 to provide the binary indication.

With respect to Appellant's arguments on the first full paragraph of page 8, Examiner responds that while the claims recite "receiving a power supply voltage as the first voltage" and "receiving a reference voltage as the second voltage", nowhere does the claim recited that the circuit is always receiving "power supply voltage as the first voltage" or that the circuit is always receiving "reference voltage as the second voltage". Clearly, the circuit receives the power supply voltage Vcc when transistor 36 is on, meeting the claim language, and the circuit receives the voltage at the drain transistor 38, meeting the claim language. Further, Appellant argues concerning the language stating "said reference voltage determining a level of an internal voltage generated from said power supply". Examiner initially points out that nowhere does the claim state where this "internal voltage" is provided. As discussed above, it is clear that the voltage on the drain of 38 determines the "voltage level" on the non-inverting input and that this voltage is an "internal voltage" generated from the "power supply voltage" Vcc.

With respect to the argument in the third and fourth full paragraphs of page 8, as stated above, the claims clearly state that the circuit produces a "difference signal" corresponding to the difference between the "first voltage" and the "second voltage", contrary to what is stated. The reference to Bion meets the claim language for the reasons discussed above.

With respect to the discussion in the last full paragraph of page 8 and the paragraph linking pages 8-9, again Examiner points out that, contradictory to Appellant's remarks, that the buffer of Bion will necessarily provide a binary output indication when the "first voltage" (at the inverting input) is higher than the "second voltage" (at the non-inverting input)" for the reasons as discussed above.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,
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Art Unit 2816

September 29, 2003

Conferees

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